REMARKS/ARGUMENTS

The Applicants respectfully request reconsideration of the rejections set forth in the Final Office Action mailed on March 8, 2006. Claim 1 has been amended. Entry of these amendments is respectfully requested. The amendments present subject matter that was originally present in claims 1 and 6; Fig 2, elements 216 and 218; page 1, lines 28-29; page 11, lines 18-31; and elsewhere. Claims 1-16 and 37-40 remain pending in this application.

TELEPHONE INTERVIEW

Examiner Shrinivas H. Rao is thanked for the courtesy of a telephone interview extended to Applicants' representative on May 2, 2006. During this interview, the rejected claims were discussed with reference to the cited art. Further clarification of the patentability of the rejected claims is provided below for the Examiner's convenience.

PATENTABILITY OF CLAIMS 1-16 AND 37-40

In the Office Action, the Examiner rejected claims 1-16 and 37-40 under 35 U.S.C. 102(b) as being anticipated by *DiStefano* (U.S. Pat. No. 6,127,724). The Applicants respectfully traverse the rejections for the reasons set forth below.

Claim 1 as amended recites a semiconductor package comprising "a die, a wire bonding packaging substrate, a plurality of interconnects, a molding interface material, and a molding cap." In particular, claim 1 recites "a die having a plurality of layers of low-K dielectric material in the die"; "a molding interface material applied to at least a portion of the top surface of the die"; and "a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material". As explained fully below, the cited art (particularly the *DiStefano* patent relied on the by Examiner) simply does not show or suggest the two separate elements of a molding interface material and a molding cap configured in the manner claimed. For example, the cited art fails to teach or suggest having the molding cap covering at least a portion of the molding interface material, which is applied to at least a portion of the top surface of the die. (See Fig. 2, elements 212 and 216) Further, the cited art clearly does not show or suggest a die having a plurality of layers of low-K dielectric material in the die. For example, the cited art fails to teach or suggest a low-K Si die or an extra low-K Si die.

The packages of the present invention include die covered with molding interface materials that can control the considerable pressures caused by the CTE mismatch between the various components in the packages. In some aspects, the packages of the present invention

include a molding interface material that is applied between the low-K Si die and the molding compound such that the molding interface material strengthens the structural integrity of the low-K Si die and/or the molding interface material redistributes the packaging stress caused by the CTE mismatch between the various components of the wire bonding package (e.g., molding compound, substrate, silicon portion of the die, low-K dielectric portion of the die, die attach pad, etc.). As such, the molding interface material provides sufficient flexibility and support to counter the inherent package stresses of the CTE mismatch (e.g., caused from temperature cycling during reliability thermal cycle testing and during industrial grade testing that ranges from –55°C to 125°C) without causing any layer of the low-K materials to delaminate or crack. (See page 7, line 26 to page 8, line 7)

DiStefano describes a semiconductor chip assembly. In particular, a semiconductor chip 32 is mounted in face-up disposition on a dielectric element 20, with thermally conductive but flexible elements 50 disposed between the chip bottom surface 36 and the top surface 22 of the dielectric element 20 so as to provide a compliant but thermally conductive path from the chip 32 to a substrate 66 which is bonded to the terminals 62. A spreader 60 having coefficient of thermal expansion substantially equal to that of the chip 32 overlies the front surface and constrains an encapsulant 58 surrounding the leads 54 so as to minimize shear deformation of the encapsulant 58. (See Abstract; FIG. 1)

In rejecting claim 1, the Examiner states that the molding interface material and the molding cap respectively correspond to Fig. 1, elements 52 and 58. As shown in Fig. 1, element 52 is underneath the semiconductor chip 32 whereas element 58 is on the top surface 34 of semiconductor chip 32. Although element 58 covers at least a portion of element 52, element 58 only covers a portion of element 52 that is underneath semiconductor chip 32. Therefore, *DiStefano* fails to teach or suggest "a molding interface material applied to at least a portion of the top surface of the die" and "a molding cap covering at least a portion of the die, packaging substrate, interconnects, and molding interface material." It is respectfully submitted that claim 1 is patentably distinct from the cited art.

Further, the Examiner states that "*DiStefano* describes a Low-K Si die and not a conventional chip or die only." (See page 8 of the Office Action) In support of this statement, the Examiner references layers 20 and 26 as being the plurality of layers of low K dielectric material. However, neither elements 20 or 26 is an integral part of semiconductor chip 32. As shown in Fig. 1, elements 20 and 26 are respectively dielectric element and conductive traces that are separate from semiconductor chip 32. Although the Examiner also states that *DiStefano* teaches using polyimide for dielectric element 20, this still does not overcome the fact that

dielectric element 20 is not part of semiconductor chip 32 but instead a separate element located outside of semiconductor chip 32. Therefore, *DiStefano* fails to teach or suggest "a die having a plurality of layers of low-K dielectric material in the die." It is again respectfully submitted that claim 1 is patentably distinct from the cited art.

The Examiner's rejections of the dependent claims are also respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 2-16 and 37-40 each depend either directly or indirectly from independent claim 1 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claim 1. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

For example, claim 3 specifies "wherein the molding interface material is polyimide." That is, the molding interface material is polyimide as opposed to the die being made of polyimide (as the Examiner alludes to on page 8 of the Office Action in supporting his statement that *DiStefano* describes a Low-K Si die and not a conventional chip or die only).

For another example, claim 6 specifies "wherein the molding interface material covers multiple non-contiguous regions on the top surface of the die." In rejecting claim 6, the Examiner references Figs. 1-7 of *DiStefano*. However, none of the Figs. 1-7 includes a molding interface material covering multiple non-contiguous regions on the top surface of the die.

In view of the above, it is respectfully requested that the Examiner withdraw the rejection of claims 1-16 and 37-40 under 35 U.S.C § 102(b). It is respectfully submitted that all pending claims are allowable and that this case is now in condition for allowance. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below. If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. **ALTRP100**).

Respectfully submitted,
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